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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/659,421	09/10/2003	2812	750	NSC1-M3200 [P05675]	3	3	3

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STALLMAN & POLLOCK LLP Suite 290 121 Spear Street San Francisco, CA 94105 RECEIVED

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**CONFIRMATION NO. 4626** 

**FILING RECEIPT** 

\*OC00000011405064\*

Date Mailed: 12/04/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)	·		
✓ Andrew Strachan, Santa Clara, CA; ✓ Vladislav Vashchenko, Palo <del>alto,</del> CA;	RIOR ART STATEMENT DUE: (Ale 1, take 12 los		
Àlto	FOREIGN FILING LETTER DUE: 03 10 04		
Domestic Priority data as claimed by applicant	FOREIGN FILING DEADLINE: 09/10/04		
Foreign Applications	13 MONTH SUSPENSE DATE: 09 100 05		

If Required, Foreign Filing License Granted: 12/02/2003

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

Method of improving the breakdown voltage of a diffused semiconductor junction

**Preliminary Class** 

438

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Andrew Strachan et al.

Application No.: 10/659,421

Filed: September 10, 2003

For: METHOD OF IMPROVING THE

BREAKDOWN VOLTAGE OF A DIFFUSED SEMICONDUCTOR

JUNCTION

Group Art Unit: 2812

Examiner: Unknown

REQUEST FOR CORRECTION OF OFFICIAL FILING RECEIPT

121 Spear Street, Suite 290 San Francisco, CA 94105

(415) 512-1312

Commissioner for Patents
Attn: Office of Initial Patent Examination's
Filing Receipt Corrections
P.O. Box 1450
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 11, 2003.

STALLMAN & POLLOCK LLP

Dated: 12/11/03

Bv

Janet Chan

Sir:

Attached is a copy of the Official Filing Receipt which was received in our offices on December 8, 2003, in connection with the above-identified application

The Official Filing Receipt is in error. Please amend the receipt as shown in red ink on the attached copy as follows:

Please amend inventor Vladislav Vashchenko's residence as follows: Palo Alto, CA.

Please forward the amended Official Filing Receipt to:

STALLMAN & POLLOCK LLP

Attn: Michael J. Pollock 121 Spear Street, Suite 290 San Francisco, CA 94105

In the event it is determined that a fee pursuant to 37 C.F.R. §1.19(h) is required in connection with this request, the Commissioner is hereby authorized to charge payment of any

Atty Docket No.: NSC1-M3200 [P05675]

fees associated with this communication or credit any overpayment to Deposit Account No. 50-1703, under Order No. NSC1-M3200. **A duplicate of this sheet is enclosed.** 

Respectfully submitted,

STALLMAN & POLLOCK LLP

Dated:  $12 \sim 11 - 2003$ 

Michael J. Pollock Reg. No. 29,098

Attorneys for Applicant(s)

Atty Docket No.: NSC1-M3200 [P05675]